FAIRCHILD SEMICONDUCTOR®

March 2008

USB1T11A — Universal Serial Bus Transceiver

Features

- Complies with Universal Serial Bus Specification 1.1
- Utilizes Digital Inputs and Outputs to Transmit and Receive USB Cable Data
- Supports 12Mbit/s “Full Speed” and 1.5Mbit/s “Low Speed” Serial Data Transmission
- Compatible with the VHDL “Serial Interface Engine” from USB Implementers' Forum
- Supports Single-ended Data Interface
- Single 3.3V Supply
- ESD Performance: Human Body Model
  >9.5kV on D-, D+ pins only
  >4kV on all other pins
- 16-lead, Space-Saving, MLP Package

Description

The USB1T11A is a one-chip, generic USB transceiver. It is designed to allow 5.0V or 3.3V programmable and standard logic to interface with the physical layer of the Universal Serial Bus. It is capable of transmitting and receiving serial data at both full-speed (12Mbit/s) and low-speed (1.5Mbit/s) data rates.

The input and output signals of the USB1T11A conform with the “Serial Interface Engine.” Implementation of the serial interface engine allows designers to make USB-compatible devices with off-the-shelf logic to modify and update the application.

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
USB1T11AM	-40 to +85°C	14-Lead, Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150-Inch Narrow	Tube
USB1T11AMX	-40 to +85°C	14-Lead, Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150-Inch Narrow	Tape and Reel
USB1T11ABQX	-40 to +85°C	16-Terminal, Molded Leadless Package (MLP), JEDEC MO-220, 3mm Square	Tape and Reel
USB1T11AMTC	-40 to +85°C	14-Lead, Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mmWide	Tube
USB1T11AMTCX	-40 to +85°C	14-Lead, Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide	Tape and Reel

All packages are lead free per JEDEC: J-STD-020B standard.

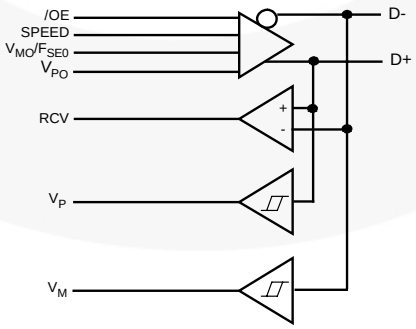


Figure 1. Logic Diagram

Pin Configuration

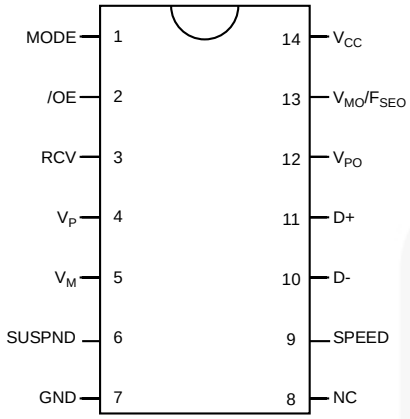


Figure 2. TSSOP and SOIC Pin Assignments

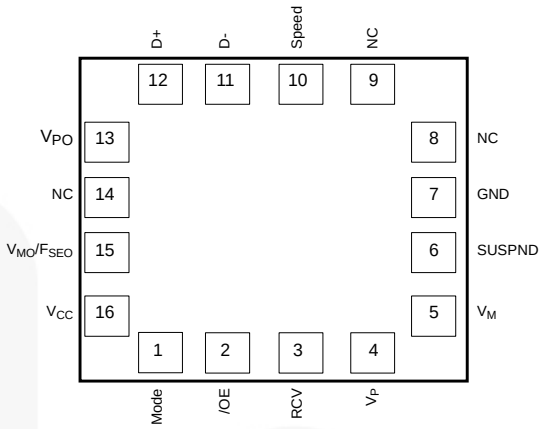


Figure 3. MLP Pin Assignments

Pin Descriptions

Pin Names	I/O	Description
RVC	O	**Receive Data**. CMOS level output for USB differential input.
/OE	I	**Output Enable**. Active LOW, enables the transceiver to transmit data on the bus. When not active, the transceiver is in receive mode.
Mode	I	**Mode**. When left unconnected, a weak pull-up transistor pulls it to V_{CC} and, in this GND, the V_{MO}/F_{SEO} pin takes the function of F_{SEO} (force SEO).
V_{PO},V_{MO}/F_{SEO}	I	Inputs to differential driver. (Outputs from SIE.)

Mode	V_{PO}	V_{MO}/F_{SEO}	RESULT
0	0		Logic “0”
	0		/SEO
	1		Logic “1”
	1		/SEO
1	0	0	/SEO
	0	1	Logic “0”
	1	0	Logic “1”
	1	1	Illegal Code

V_P,V_M	O	Gated version of D- and D+. Outputs are logic “0” and logic “1.” Used to detect single ended zero (/SEO), error conditions, and interconnected speed. (Input to SIE).

V_P	V_M	RESULT
0	0	/SEO
0	1	Low Speed
1	0	Full Speed
0	1	Error

D+, D-	AI/O	Data+, Data-. Differential data bus conforming to the Universal Serial Bus standard.
SUSPND	I	**Suspend**. Enables a low-power state while the USB bus is inactive. While the suspend pin is active, it drives the RCV pin to a logic “0” state. Both D+ and D- are 3-STATE.
Speed	I	**Edge Rate Control**. Logic “1” operates at edge rates for “full speed.” Logic “0” operates edge rates for “low speed.”
V_{CC}		3.0 to 3.6 power supply.
GND		Ground reference.

Functional Truth Table

Input					I/O		Outputs			
Mode	V_{PO}	V_{MO}/F_{SEO}	/OE	SUSPND	D+	D-	RCV	V_P	V_M	Result
0	0	0	0	0	0	1	0	0	1	Logic “0”
0	0	1	0	0	0	0	Undefined State	0	0	/SEO
0	1	0	0	0	1	0	1	1	0	Logic “1”
0	1	1	0	0	0	0	Undefined State	0	0	/SEO
1	0	0	0	0	0	0	Undefined State	0	0	/SEO
1	0	1	0	0	0	1	0	0	1	Logic “0”
1	1	0	0	0	1	0	1	1	0	Logic “1”
1	1	1	0	0	1	1	Undefined State	Undefined State	Undefined State	Illegal Code
Don’t Care	Don’t Care	Don’t Care	1	0	3-State	3-State	Undefined State	Undefined State	Undefined State	D+/D- Hi-Z
Don’t Care	Don’t Care	Don’t Care	1	1	3-State	3-State	Undefined State	Undefined State	Undefined State	D+/D- Hi-Z

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	DC Supply Voltage		0.5	7.0	V
I_{IK}	DC Input Diode Current, V_{IN}<0V			-50	mA
V_{IN}	Input Voltage(1)		0.5	5.5	V
$V_{I/O}$	Input Voltage		0.5	V_{CC} + 0.5	V
I_{OK}	Output Diode Current, V_O>V_{CC} or V_O<0			±50	mA
V_O	Output Voltage		0.5	V_{CC} + 0.5	V
I_O	Output Source or Sink Current (V_O = 0 to V_{CC})	V_P, V_M, RCV Pins		±15	mA
		D+/D- Pins		±50	
I_{CC} / I_{GND}	V_{CC} / GND Current			±100	mA
T_{STG}	Storage Temperature Range		-60	+150	°C

Note:

1. The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Power Supply Operating	3.0	3.6	V
V_{IN}	Input Voltage	0	5.5	V
$V_{AI/O}$	Input Range for AI/0	0	V_{CC}	V
V_O	Output Voltage	0	V_{CC}	V
T_A	Operating Ambient Temperature, Free Air	-40	+85	°C

DC Electrical Characteristics Digital Pins

Over recommended range of supply voltage and operating free air temperature unless otherwise noted.
V_{CC} = 3.0V to 3.6V.

Symbol	Parameter	Conditions	T_A=-40 to +85°C			Units
			Min.	Typ.	Max.	
Input Levels						
V_{IL}	Low-Level Input Voltage				0.8	V
V_{IH}	High-Level Input Voltage		2			V
Output Levels						
V_{OL}	Low-Level Output Voltage	I_{OL}=4mA			0.4	V
		I_{OL}=20µA			0.1	
V_{OH}	High-Level Output Voltage	I_{OH}=4mA	2.5			V
		I_{OH}=20µA	V_{CC}-0.1			
Leakage Current						
I_{IN}	Input Leakage Current	V_{CC}=3.0 to 3.6			±5	µA
I_{CCFS}	Supply Current, Full Speed	V_{CC}=3.0 to 3.6			5	mA
I_{CCLS}	Supply Current, Low Speed	V_{CC}=3.0 to 3.6			5	mA
I_{CCQ}	Quiescent Supply Current	V_{CC}=3.0 to 3.6, V_{IN}=V_{CC} or GND			5	mA
I_{CCS}	Supply Current in Suspend	V_{CC}=3.0 to 3.6 Mode=V_{CC}			10	µA

DC Electrical Characteristics D+/D- Pins

Over recommended range of supply voltage and operating free air temperature unless otherwise noted.
V_{CC} = 3.0V to 3.6V.

Symbol	Parameter	Conditions	T_A=-40 to +85°C			Units
			Min.	Typ.	Max.	
Input Levels						
V_{DI}	Differential Input Sensitivity	|(D+) – (D-)|	0.2			V
V_{CM}	Differential Common-Mode Range	Includes V_{DI} Range	0.8		2.5	V
V_{SE}	Single-Ended Receiver Threshold		0.8		2.0	V
Output Levels						
V_{OL}	Static Output Low-Voltage				0.3	V
V_{OH}	Static Output High-Voltage	R_L of 1.5kΩ to 3.6V	2.8		3.6	V
V_{CR}	Differential Crossover	R_L of 1.5kΩ to GND	1.3		2.0	V
Leakage Current						
I_{OZ}	High Z-State Data Line Leakage Current	0V<V_{IN}<3.3V			±5	µA
Capacitance						
C_{IN}(2)	Transceiver Capacitance	Pin to GND			10	pF
	Capacitance Match				10	%
Output Resistance						
Z_{DRV}(3)	Driver Output Resistance	Steady-State Drive	4		20	Ω
	Resistance Match				10	%

Notes:

2. This specification is guaranteed by design and statistical process distribution.
3. Excludes external resistor. To comply with USB specification 1.1, external series resistors of 24W ±1% each on D+ and D- are recommended.

AC Electrical Characteristics D+/D- Pins, Full Speed

Over recommended range of supply voltage and operating free air temperature unless otherwise noted.
V_{CC} = 3.0V to 3.6V, C_L = 50Pf; R_L = kΩ on D+ to V_{CC}.

Symbol	Parameter	Conditions	T_A=-40 to +85°C			Units
			Min.	Typ.	Max.	
Driver Characteristics						
t_R, t_F	Rise and Fall Time	10 and 90%, Figure 4	4		20	ns
t_{RFM}	Rise/Fall Time Matching	t_r / t_f	90		110	%
V_{CRS}	Output Signal Crossover Voltage		1.3		2.0	V
Driver Timings						
t_{PLH}	Driver Propagation Delay (V_{PO},V_{MO}/F_{SEO} to D+D-)	Figure 5			18	ns
t_{PHZ}, t_{PLZ}	Driver Disable Delay (/OE to D+/D-)	Figure 7			13	ns
t_{PZH}, t_{PZL}	Driver Enable Delay (/OE to D+/D-)	Figure 7			17	ns
Receiver Timings						
t_{PLH}	Receiver Propagation Delay	Figure 6			16	ns
t_{PHL}	D+/D- to RVC	Figure 6			19	ns
t_{PLH}, t_{PHL}	Single-ended Receiver Delay (D+,D- to V_P, V_M)	Figure 6			8	ns

AC Electrical Characteristics D+/D- Pins, Low Speed

Over recommended range of supply voltage and operating free air temperature unless otherwise noted.
V_{CC} = 3.0V to 3.6V, C_L = 200pF to 600pF; R_L = 1.5kΩ on D- to V_{CC}.

Symbol	Parameter	Conditions	T_A=-40 to +85°C			Units
			Min.	Typ.	Max.	
Driver Characteristics						
t_{LR}, t_{LF}	Rise and Fall Time	10 and 90%, Figure 4	75		300	ns
t_{RFM}	Rise/Fall Time Matching	t_r / t_f	80		120	%
V_{CRS}	Output Signal Crossover Voltage		1.3		2.0	V
Driver Timings						
t_{PLH}, t_{PHL}	Driver Propagation Delay (V_{PO},V_{MO}/F_{SEO} to D+D-)	Figure 5			300	ns
t_{PHZ}, t_{PLZ}	Driver Disable Delay (/OE to D+/D-)	Figure 7			13	ns
t_{PZH}, t_{PZL}	Driver Enable Delay (/OE to D+/D-)	Figure 7			205	ns
Receiver Timings						
t_{PLH}, t_{PHL}	Receiver Propagation Delay (D+/D- to RVC)	Figure 6			18	ns
t_{PLH}, t_{PHL}	Single-ended Receiver Delay (D+,D- to V_P, V_M)	Figure 6			28	ns

AC Loadings and Waveforms

V_{OL} and V_{OH} are the typical output voltage drops that occur with the output load. V_{CC} never goes below 3.0V.

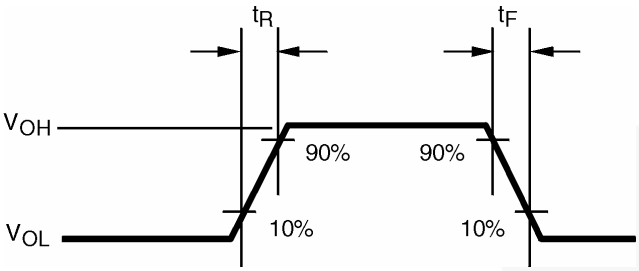


Figure 4. Rise and Fall Times

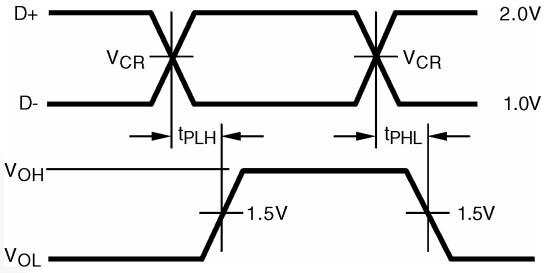


Figure 5. V_{PO}, V_{MO}/F_{SEO} to D+/D-

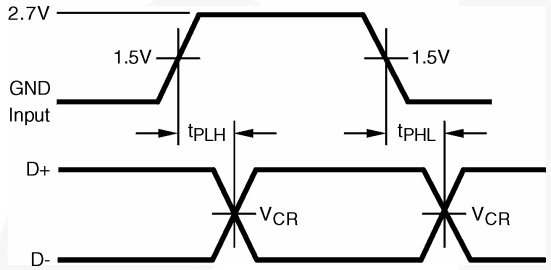


Figure 6. D+/D- to RCV, V_P/VM

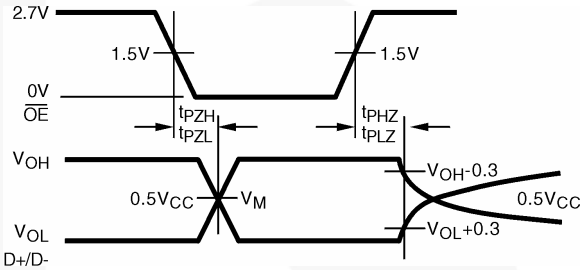


Figure 7. /OE to D+/D-

Test Circuits and Waveforms

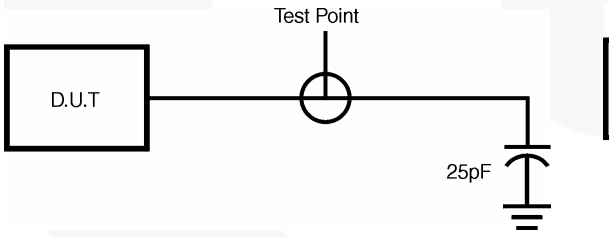


Figure 8. Load for V_M/V_P and RCV

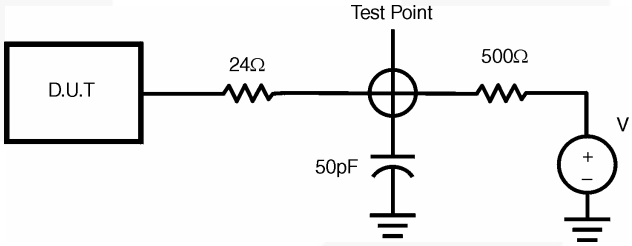
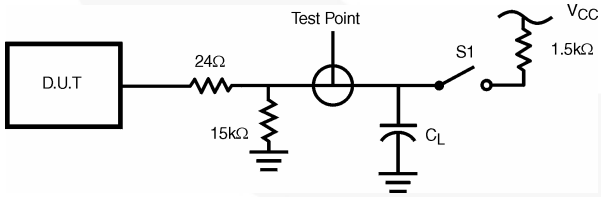


Figure 9. Load for Enable and Disable Times



Test	S1
D-/LS	Close
D+/LS	Open
D-/FS	Open
D+/FS	Close

C_L=50pF, Full Speed
C_L=200pF, Full Speed (Minimum Timing)
C_L=600pF, Full Speed (Maximum Timing)
1.5kΩ on D-(Low Speed) or D+ (Full Speed) only.

Figure 10. Load for D+/D-

Physical Dimensions

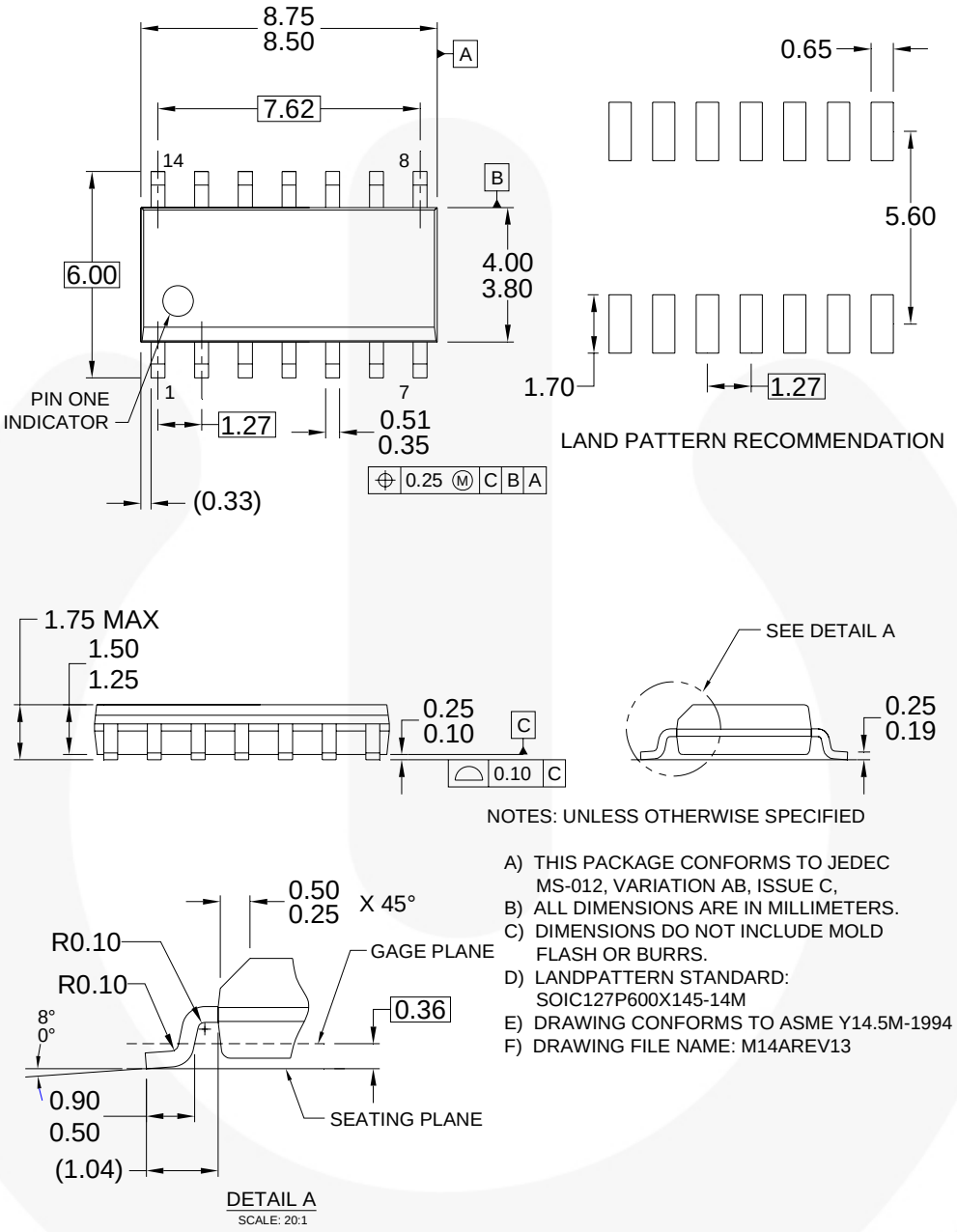


Figure 11. 14-Lead, Small Outline Integrated Circuit (SOIC) MO-012, 0.150-inch Wide

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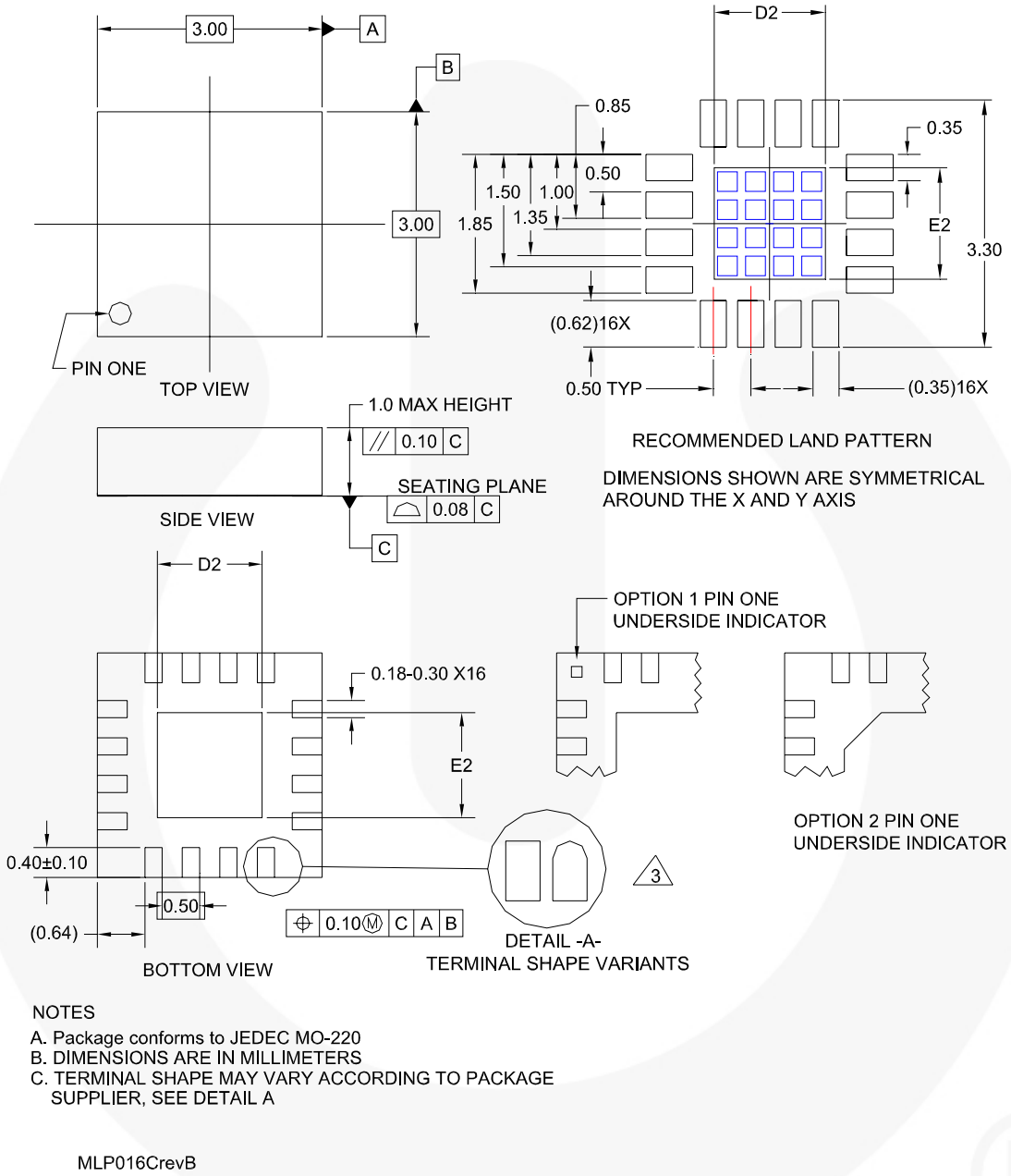
Physical Dimensions



NOTES

A. Package conforms to JEDEC MO-220
B. DIMENSIONS ARE IN MILLIMETERS
C. TERMINAL SHAPE MAY VARY ACCORDING TO PACKAGE SUPPLIER, SEE DETAIL A

MLP016CrevB

Figure 12. 16-Terminal, Molded Leadless Package (MLP), JEDEC MO-220, 3mm Square

Click here for tape and reel specifications, available at:

http://www.fairchildsemi.com/products/analog/pdf/MLP6_3x3_TNR.pdf

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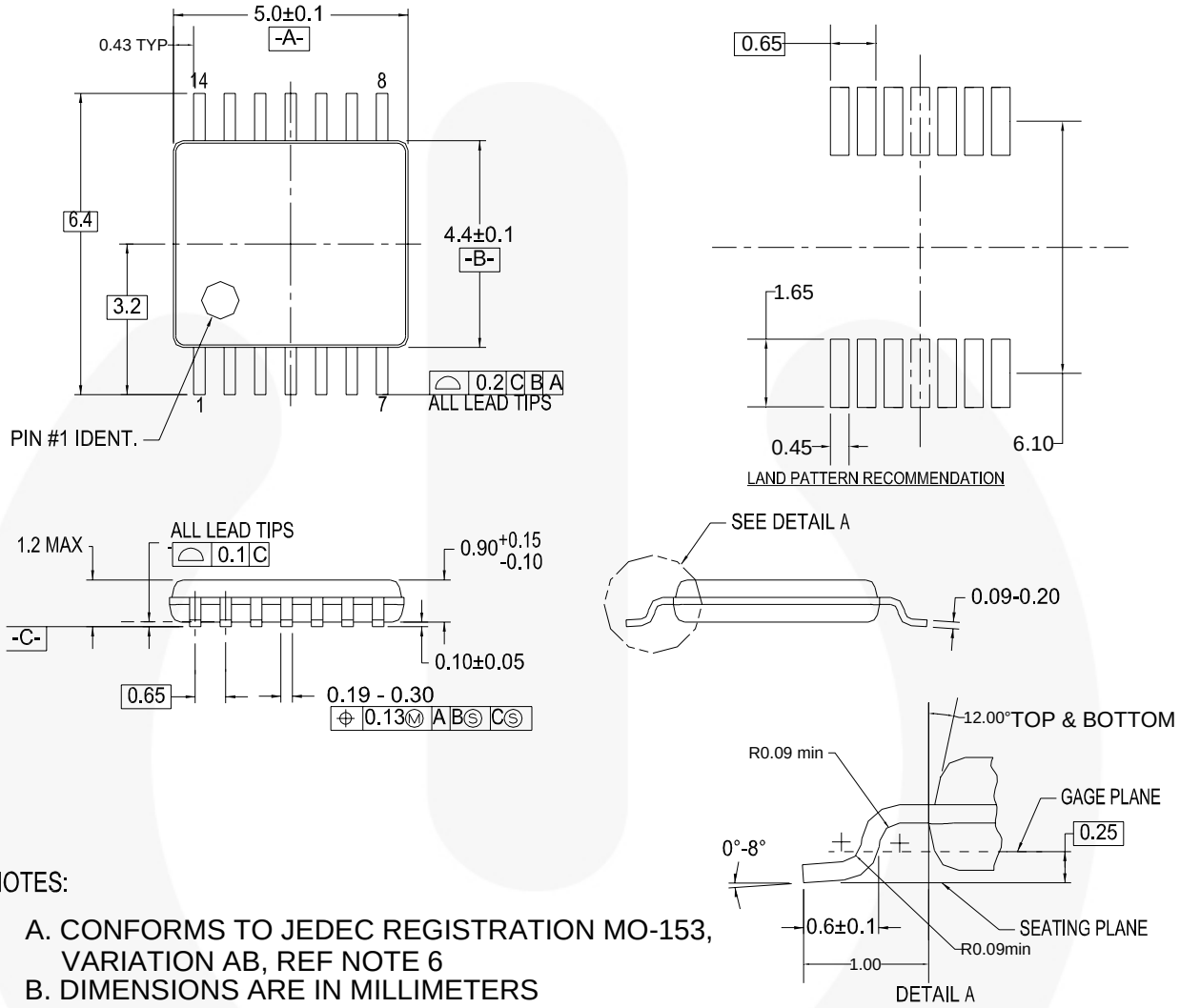
Physical Dimensions



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6

B. DIMENSIONS ARE IN MILLIMETERS

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982

E. LANDPATTERN STANDARD: SOP65P640X110-14M

F. DRAWING FILE NAME: MTC14REV6

Figure 13. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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Green FPS™ e-Series™
GTO™
IntelliMAX™
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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	This datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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